PATENT Docket No.:JCLA4280-D2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	MING-DOU KER et al.	)
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Filed:	Herewith	)
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For:	LOW-CAPACITANCE BONDING PAD FOR SEMICONDUCTOR DEVICE	)
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PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination on merits, please amend the above-identified application as follows:

IN THE SPECIFICATION:

On page 1, lines 5-7, please replace "This application claims the priority benefit of Taiwan application serial no. 88104304, filed March 19, 1999, the full disclosure of which is incorporated herein by reference." with --This application is a divisional application of, and claims the priority benefit of, U.S. application serial No. 09/329,648 filed on June 09, 1999.--

IN THE CLAIMS:

Please cancel claims 1-25.

Please add the following new claims:

26. (Newly Added) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one and other by a plurality of via plugs in the dielectric layers;

an uppermost metal layer positioned on the stack, wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer; and

a passivation layer having a bonding pad opening positioned on the uppermost metal layer for externally electric connection.

27. (Newly Added) The low-capacitance bonding pad of claim 1, wherein the metal layers in the stack are in a concentric circle arrangement.

28. (Newly Added) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one and other by a plurality of via plugs in the dielectric layers and are in a concentric circle arrangement;

an uppermost metal layer positioned on the stack; and

a passivation layer having a bonding pad opening on the uppermost metal layer for externally electric connection.

29. (Newly Added) The low-capacitance bonding pad of claim 28, wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer.

30. (Newly Added) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region; and

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, wherein the bonding pad being aligned with the doped region.

31. (Newly Added) The low-capacitance bonding pad of claim 30, wherein the type of the ions doped in the doped region is opposite to those in the well.

32. (Newly Added) The low-capacitance bonding pad of claim 30, wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer.

33. (Newly Added) The low-capacitance bonding pad of claim 30, wherein the metal layers in the stack are in a concentric circle arrangement.

34. (Newly Added) The low-capacitance bonding pad of claim 30, wherein two adjacent metal layers are aligned with each other in the stack.

35. The low-capacitance bonding pad of claim 30, wherein two adjacent metal layers are not aligned with each other in the stack.

36. (Newly Added) A semiconductor, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region; and

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, wherein the bonding pad is aligned with the doped region, and wherein the metal layers in the stack are in a concentric circle arrangement; and

a device under the bonding pad.

37. (Newly Added) The semiconductor of 36, wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer.

38. (Newly Added) The semiconductor of claim 36, wherein the type of the ions doped in the doped region is opposite to those in the well.

39. (Newly Added) A semiconductor, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region; and

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, wherein the bonding pad is aligned with the doped region; and wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer; and

a device under the bonding pad.

40. (Newly Added) The semiconductor of claim 39, wherein the metal layers in the stack are in a concentric circle arrangement.

41. (Newly Added) The semiconductor of claim 39, wherein the type of the ions doped in the doped region is opposite to those in the well.

Respectfully submitted,

Dated: 3/27/2001

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